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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,974	01/15/2004	Jenoe Tihanyi	1890-0033	4260

7590 03/31/2008

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
03/31/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,974	TIHANYI, JENOE	
	Examiner	Art Unit	
	HIEP NGUYEN	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15 and 18-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15 and 18-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 15, 18, 19, 20 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirano Yoji (JP, 06-053800). See attachment.

Regarding claims 15 and 19, figure 1 of Hirano shows a MOSFET circuit comprising:

a first MOS transistor (Q3) having a first number of cells (N1),

a second MOS transistor (Q1) having a second number of cells (N2), the second number being less than the first number and the second MOS transistor being provided with a source-drain path in parallel with a source-drain path of the first MOS transistor between a voltage source and reference potential, and

a Zener diode (SBD1) coupled between a gate of the first MOS transistor (Q3) and a gate of the second MOS transistor (Q1), wherein the Zener diode is further coupled between the gate of the second MOS transistor (Q1) and a control input (3) of the MOSFET circuit, and wherein the Zener diode is forward biased from the control input to the gate of the second transistor (Q1). It is inherent that the second number (N2) is less than the first number (N1) because transistor (Q1) is smaller than transistor (Q3) (see abstract), the number of cells (N2) is smaller than the number of cells (N1). (see 7,235,842; 4,931,844). The first resistor is resistor (R1).

Regarding claim 18, the second resistor is resistor (R2).

Regarding claim 20, because the circuit of Hirano is an IC circuit, it is inherent that the Zener diode and the first resistor are integrated with one another.

Regarding claims 24, figure 1 of Hirano shows a MOSFET circuit comprising:

a first MOS transistor (Q3) having a first number of cells (N1), the first MOS transistor integrated into a semiconductor body;

a second MOS transistor (Q1) having a second number of cells (N2), the second MOS transistor integrated into the semiconductor body, the second number being less than the first number and the second MOS transistor being provided with a source-drain path in parallel with a source-drain path of the first MOS transistor between a voltage source and reference potential, and a Zener diode (SBD1) coupled between a gate of the first MOS transistor (Q3) and a gate of the second MOS transistor (Q1), wherein the Zener diode is further coupled between the gate of the second MOS transistor (Q1) and a control input (3) of the MOSFET circuit, and wherein the Zener diode is forward biased from the control input to the gate of the second transistor (Q1). It is inherent that the second number (N2) is less than the first number (N1) because transistor (Q1) is smaller than transistor (Q3) (see abstract), the number of cells (N2) is smaller than the number of cells (N1). (see 7,235,842; 4,931,844). The first resistor is resistor (R1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18, 21-23, and 25-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano Yoji (JP, 06-053800) in view of Sendelweck (US 5,045,733), Pavlin et al. (US 5,438,285), Herfurth et al. (US 2003/0089980), Ahlers et al. (6,667,514), Zivic (US 6,444,504) and Kuma (US 6,855,981).

Regarding claim 18, figure 1 of Hirano includes all the limitations of this claim except for the limitation that there is a second resistor connected in series with a parallel formed by

the Zener diode and the first resistor. Figure 1 of Sendelweck shows a resistor (28) connected is series with a Zener diode for precisely biased the Zener diode (col. 5, lines 67-68 and col. 6 lines 1-2).

Regarding claims 21, 22, 23 and 32, the technique of fabrication of the zener diode and the resistor are well known in the art and is fully shown by Kumar (6,855, 981, col. 11, lines 24-30). Kumar does not show that "the dope concentration of the highly doped layer is less than 10exp 19 charge carrier cm –exp 3". However, it is old and well known and it would have been an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative predetermined value of a differential input voltage limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative predetermined value of a differential input voltage. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990) as set forth in MPEP 2144.05(III). Therefore, it would have been obvious to one having ordinary skill in the art to select the dope concentration of the highly doped layer to be less than 10exp19 charge carrier cm –exp 3" dependent upon particular environment of use to ensure optimum performance.

Regarding claims 25-28, figure 1 of Hirano includes all the limitations of this claim except for the limitation about the special sizes of the transistors. Figure 2 and column 4, lines 23-40 of the reference of Pavlin shows that the transistors of the circuit can have different

number of cells or different sizes. Paragraph [0029] of Herfurth shows that coolMOS transistor can stand high voltage. It would have been an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative resistance values limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative resistance values limitations. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III). Therefore, it would have been obvious to one of ordinary skill in the art to select special type of transistor (coolMOS for high voltage, high power, 2003/0089980) or special number of cells in each transistor, or in other words, the relative sizes of transistors in the circuit dependent upon particular environment of use to ensure optimum performance. (see Herfurth, paragraph [0008].

Regarding claim 29, figure 1 of Hirano includes all the limitations of this claim except for the limitation that the semiconductor body is of a second conduction type and charge compensation regions of a first conduction type are incorporated into the semiconductor body. Ahlers shows a semiconductor component with a charge compensation structure for providing an electrical parameter such as the on resistance of the on resistance of the semiconductor component can be substantially improve without influencing or impairing further parameter (abstract). Therefore, it would have been obvious to one of ordinary skill in the art to replace

the MOSFETs in the circuit of Hirano with the MOSFETs with a charge compensation structure taught by Ahlers for providing an electrical parameter such as the on resistance of the on resistance of the semiconductor component can be substantially improve without influencing or impairing further parameter.

Regarding claim 30, figure 1 of Hirano shows an integrated MOSFET circuit comprising:

a first MOS transistor (Q2) having a first number of cells (N1),

a second MOS transistor (Q4) having a second number of cells (N2), the second number being less than the first number and the second MOS transistor being provided with a source-drain path in parallel with a source-drain path of the first MOS transistor between a voltage source and reference potential, and

a Zener diode (SBD2) coupled between a gate of the first MOS transistor and a gate of the second MOS transistor. Hirano does not shows that the Zener diode comprising a polycrystalline layer. Zivic (abstract) shows that polycrystalline diode protects against electrostatic discharge, over current, and over surge. Therefore, it would have been obvious to one of ordinary skill in the art the replace the zener diode of Hirano with the polycrystalline diode taught by Zivic for protecting against electrostatic discharge, over current, and over surge.

Regarding claim 31, the resistor is element (R2). Kuma, col. 11, shows that the resistor can be formed by the pn junction between the polycrystalline layer and the zone.

Regarding claims 32-34, figure 1 of Hirano includes all the limitations of these claims except for the limitation that the doping concentration of the zone is less than 10^{19}charge carriers cm^3, the first number of cells is at least twice the second number of cells and the first number of cells is at least ten times the second number of cells. It would have been an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative resistance values limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical,

and it appears prima facie that the process would possess utility using another relative resistance values limitations. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III). Therefore, it would have been obvious to one having ordinary skill in the art to select the doping concentration of the zone is less than 10^{19} charge carriers cm^3, the first number of cells is at least twice the second number of cells and the first number of cells is at least ten times the second number of cells dependent upon particular environment of use to ensure optimum performance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richard N can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/

Primary Examiner, Art Unit 2816

/Hiep Nguyen/

Examiner, Art Unit 2816

Searching PAJ

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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 06-053800
(43)Date of publication of application : 25.02.1994

(51)Int.Cl. H03K 17/687
H03K 17/16

(21)Application number : 04-225188
(22)Date of filing : 31.07.1992

(71)Applicant : NEC CORP
(72)Inventor : HIRANO YOJI

(54) OUTPUT CIRCUIT

(57)Abstract:

PURPOSE: To obtain an output circuit comprising a semiconductor integrated circuit in which power supply noise at the time of an output change is reduced and the circuit is stably operated on a DC load.

CONSTITUTION: Transistors(TRs) Q3, Q4 having a larger conduction resistance and TRs Q1, Q2 having a smaller conduction resistance are connected in parallel, an input terminal 3 is directly connected to the TRs Q3, Q4 having a larger conduction resistance and the input terminal 3 is connected to the TRs Q1, Q2 having a smaller conduction resistance via delay circuits (comprising SBD1, R1 and SBD2, R2). When an input (that is, an output) is changed, the TRs having a larger conduction resistance are conductive to reduce power supply noise, and when an output level reaches a final level, the TRs having a smaller conduction resistance are conductive to increase the drive capability for a DC load thereby realizing the stable operation for the DC load.